

# FAN5631/FAN5632 Regulated Step-Down Charge Pump DC/DC Converter

## Features

- 90% Peak Efficiency
- Low EMI
- Low Ripple
- Selectable Output Voltage 1.2V/1.5V for FAN5631
- Efficiency Optimizer Feature for FAN5632
- Input Voltage Range: 2.2V to 5.5V
- Output Current: Up to 250mA
- ±5% Output Voltage Accuracy
- 30µA Operating Current
- $I_{CC} < 1\mu A$  in Shutdown Mode
- 1.7MHz Operating Frequency
- Shutdown Isolates Output from Input
- Soft-Start Limits In-Rush Current
- Short Circuit and Over Temperature Protection
- Minimum External Component Count
- Available in a 3x3mm 10-Lead MLP Package

## Applications

- Cell Phones
- Handheld Computers
- Portable Electronic Equipment
- Core Supply to Next Generation Processors
- Low Voltage DC Bus
- Digital Cameras
- DSP Supplies

## Description

The FAN5631/FAN5632 is an advanced, third-generation switched capacitor step-down DC/DC converter utilizing Fairchild's proprietary ScalarPump™ technology. This innovative architecture utilizes scalar switch re-configuration and fractional switching techniques to produce low output ripple, lower ESR spikes, and improve efficiency over a wide load range.

The FAN5631/FAN5632 produces a fixed regulated output voltage from an input voltage of 2.2V to 5V. Customized output voltages are available in 100mV increments from 1V to 1.8V. Contact a Fairchild sales representative for customized output voltage options.

In order to maximize efficiency, the FAN5631/5632 achieves regulation by skipping pulses. Depending upon load current, the size of the switches are scaled dynamically; consequently, current spikes and EMI are minimized. An internal soft-start circuitry prevents excessive current drawn from the supply. The device is internally protected against short circuit and over temperature conditions.

The FAN5631 has a dual output voltage feature. When  $V_{SEL}$  is high,  $V_{OUT}$  is 1.5V and when  $V_{SEL}$  is low,  $V_{OUT}$  is 1.2V. Other output voltage options are available upon request.

In addition, the FAN5632 has an efficiency optimizer feature that, when enabled, changes the switch mode configuration from 2:1 to 1:1 at the lower threshold of  $V_{IN}$ . The efficiency is then maintained at its peak level over a wider range of input voltages. In addition,  $V_{OUT}$  will vary between 1.2V to 1.5V as a result of this efficiency optimization. If the efficiency optimizer is not enabled,  $V_{OUT}$  is regulated to 1.5V.

Both the FAN5631 and FAN5632 are available in a 3x3mm 10-lead MLP package.

## Ordering Information

Product Number	Package Type	Order Code
FAN5631	3x3mm 10-Lead MLP	FAN5631MPX
FAN5632	3x3mm 10-Lead MLP	FAN5632MPX

## Typical Application

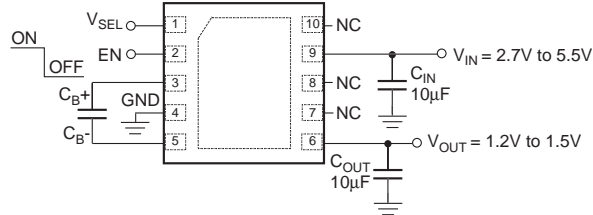
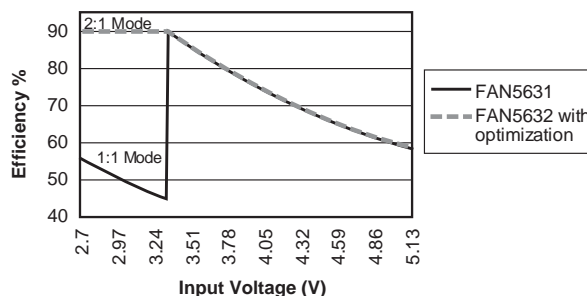


Figure 1. Typical Application



Average Efficiency (over  $V_{IN} = 2.7V$  to  $5V$ ) = 66%, With optimization = 77%  
 Average Efficiency (over  $V_{IN} = 2.7V$  to  $4.2V$ ) = 67%, With optimization = 84%

Figure 2. Typical Efficiency Graph

## Pin Assignment

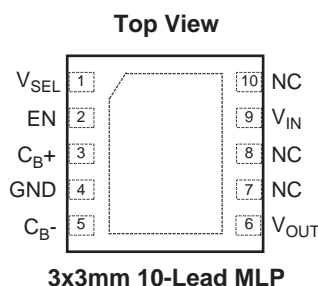


Figure 3. Pin Assignment

## Pin Description

Pin No.	Pin Name	Pin Description
1	$V_{SEL}$	<b>Output Voltage Select Logic Input Pin.</b> The $V_{SEL}$ pin can not be left floating and must be connected to either a logic high or logic low level. <b>FAN5631:</b> If a logic low is applied to the $V_{SEL}$ pin then $V_{OUT}$ is 1.2V. If a logic high is applied then $V_{OUT}$ is 1.5V. <b>FAN5632:</b> If a logic low is applied to the $V_{SEL}$ pin, the efficiency optimization mode is enabled, and the output voltage accuracy is relaxed in order to meet optimum efficiency. However, if a logic high is applied, the device will operate like a typical charge pump converter.
2	EN	<b>Enable Input Pin.</b> If a logic high is applied to the EN pin, the device is enabled. However, if a logic low is applied, the device is disabled and the supply current is reduced to less than 1µA. The EN pin can not be left floating and must be connected to either a logic high or logic low level.
3	$C_{B+}$	<b>Bucket Capacitor Positive Pin.</b>
4	GND	<b>Ground Pin.</b> This pin is connected to the internal MOSFET switches. This pin must be externally connected to GND.
5	$C_{B-}$	<b>Bucket Capacitor Negative Pin.</b>
6	$V_{OUT}$	<b>Output Voltage Pin.</b>
7	NC	<b>Not Connected.</b> This pin is not internally connected.
8	NC	<b>Not Connected.</b> This pin is not internally connected.
9	$V_{IN}$	<b>Supply Voltage Input.</b>
10	NC	<b>Not Connected.</b> This pin is not internally connected.

**Absolute Maximum Ratings** (Note1)

Parameter	Min	Max	Unit
$V_{IN}$ to GND	-0.3	6	V
All other pins to GND	-0.3	$V_{IN} + 0.3V$	V
Load Current		0.5	A
Thermal Resistance-Junction to Tab ( $\theta_{JC}$ ), 3mmx3mm 10-lead MLP (Note 2)		8	°C/W
Lead Soldering Temperature (10 seconds)		260	°C
Storage Temperature	-65	150	°C
Junction Temperature	-40	150	°C
Electrostatic Discharge (ESD) Protection Level (Note 3)	HBM	2.5	kV
	CDM	2	

**Recommended Operating Conditions**

Parameter	Min	Typ	Max	Unit
Supply Voltage Range	2.2		5.5	V
Output Current ( $V_{IN} > 2.7V$ )			250	mA
Operating Ambient Temperature Range	-40	25	+85	°C

**Notes:**

- Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to AGND.
- Junction to ambient thermal resistance,  $\theta_{JA}$ , is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics. The estimated value for zero air flow at 0.5W is 60°C/W.
- Using Mil Std. 883E, method 3015.7(Human Body Model) and EIA/JESD22C101-A (Charge Device Model).

## Electrical Characteristics

$V_{IN} = 2.2V$  to  $5.5V$ ,  $I_{OUT} = 1mA$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$ ,  $C_B = 1\mu F$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ .

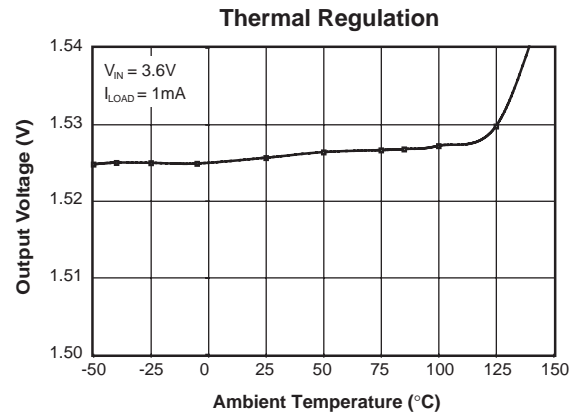
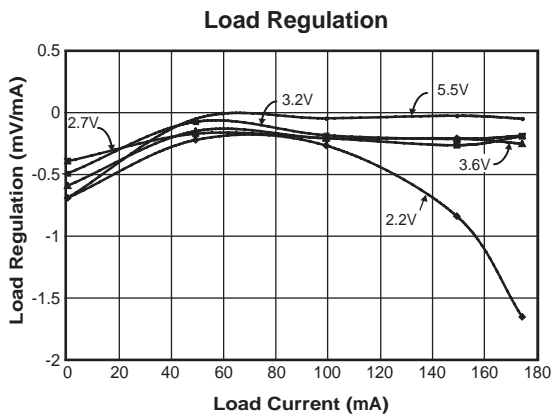
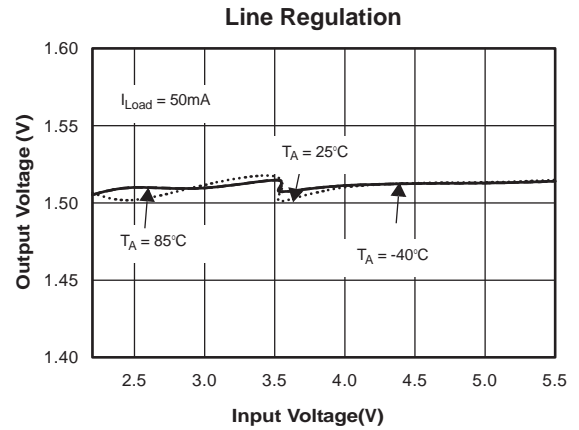
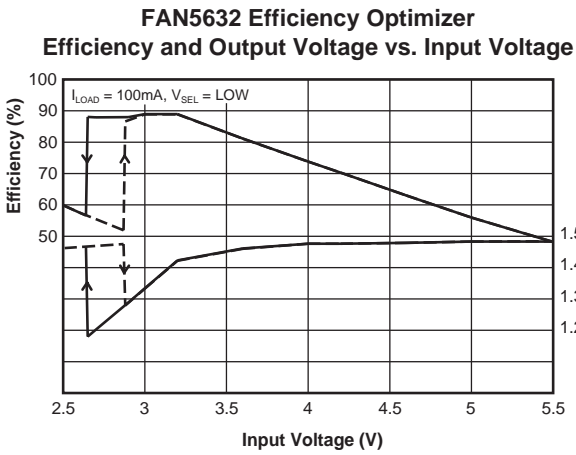
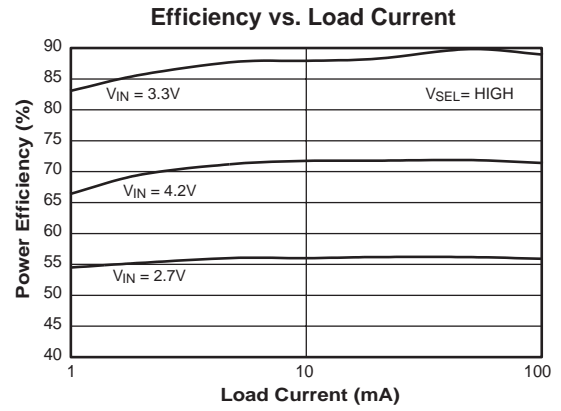
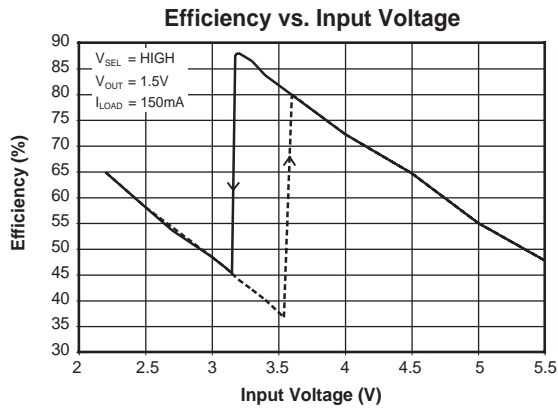
Parameter	Conditions	Min.	Typ.	Max.	Units
Input Under-Voltage Lockout			2		V
No Load Supply Current	No switching			60	$\mu A$
Output Voltage	FAN5631, SEL to HIGH		1.5		V
	FAN5631, SEL to LOW		1.2		
	FAN5632, SEL to HIGH		1.5		
	FAN5632, SEL to LOW		Variable between 1.5 and 1.2		
Output Voltage Accuracy	$1mA \leq I_{OUT} \leq 150mA$ , $V_{IN} = 2.7V$ to $5.5V$	-5		+5	%
Load Regulation	$0mA \leq I_{OUT} \leq 150mA$ , $V_{IN} = 3.6V$		0.25	1	mV/mA
Line Regulation	$I_{OUT} = 0.1mA$		0.2	4	mV/V
Shutdown Supply Current	$V_{EN} = 0V$		0.1	1	$\mu A$
Output Short Circuit Current (Note 4)	$V_{OUT} \leq 150mV$		25		mA
Peak Efficiency			90		%
$V_{IN}$ at Configuration Change	$V_{IN}$ decreasing		$2.22 \times V_{OUT}$		V
Oscillator Frequency	$V_{IN} = 3.6V$ , $I_{OUT} = 150mA$		1.7		MHz
Thermal Shutdown Threshold			150		$^{\circ}C$
Thermal Shutdown Threshold Hysteresis			15		$^{\circ}C$
Enable Logic Input High Voltage, $V_{IH}$		1.3			V
Enable Logic Input Low Voltage, $V_{IL}$				0.4	V
Enable Logic Input Current		-1		1	$\mu A$
$V_{SEL}$ Logic Input High Voltage, $V_{IH}$		1.3			V
$V_{SEL}$ Logic Input Low Voltage, $V_{IL}$				0.4	V
$V_{SEL}$ Logic Input Current		-1		1	$\mu A$
$V_{OUT}$ Turn On Time			1.6		mS

### Notes:

- The short circuit protection is designed to protect against pre-existing short circuit conditions, i.e. assembly shorts that exist prior to device power-up. The short circuit current limit is  $25mA_{Average}$ . Short circuit currents in normal operation are inherently limited by the ON-resistance of the internal FET. Since this resistance is in the range of  $1\Omega$ , in some cases thermal shutdown may occur. However, immediately following the first thermal shutdown event, the short circuit condition will be treated as pre-existing, and the load current will reduce to  $25mA_{Average}$ .

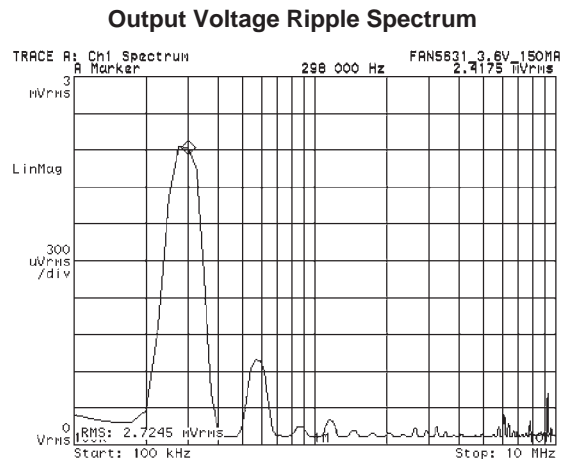
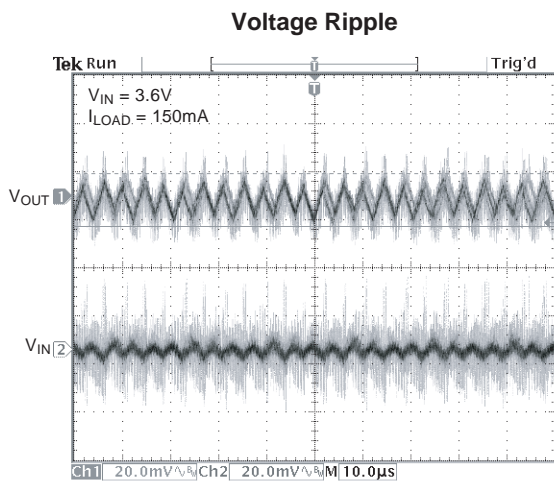
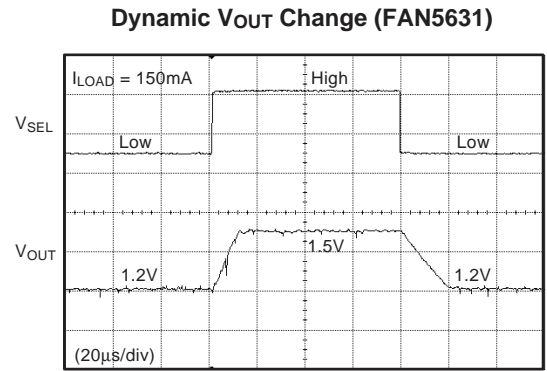
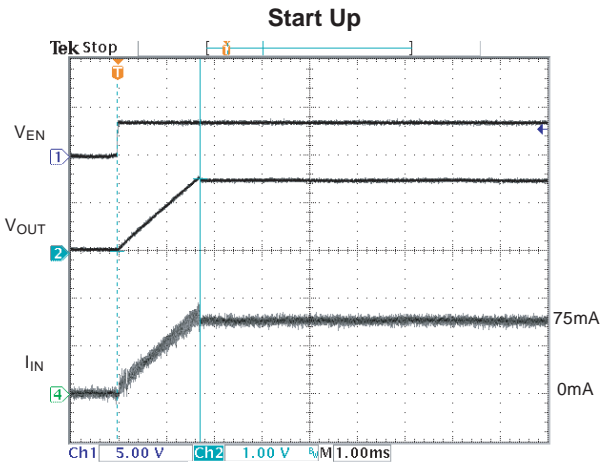
## Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{OUT} = 1.5\text{V}$ ,  $V_{IN} = 3.6\text{V}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_{OUT} = 10\mu\text{F}$ ,  $C_B = 1\mu\text{F}$ , unless otherwise noted.



### Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{OUT} = 1.5\text{V}$ ,  $V_{IN} = 3.6\text{V}$ ,  $C_{IN} = 10\mu\text{F}$ ,  $C_{OUT} = 10\mu\text{F}$ ,  $C_B = 1\mu\text{F}$ , unless otherwise noted.



## Block Diagram

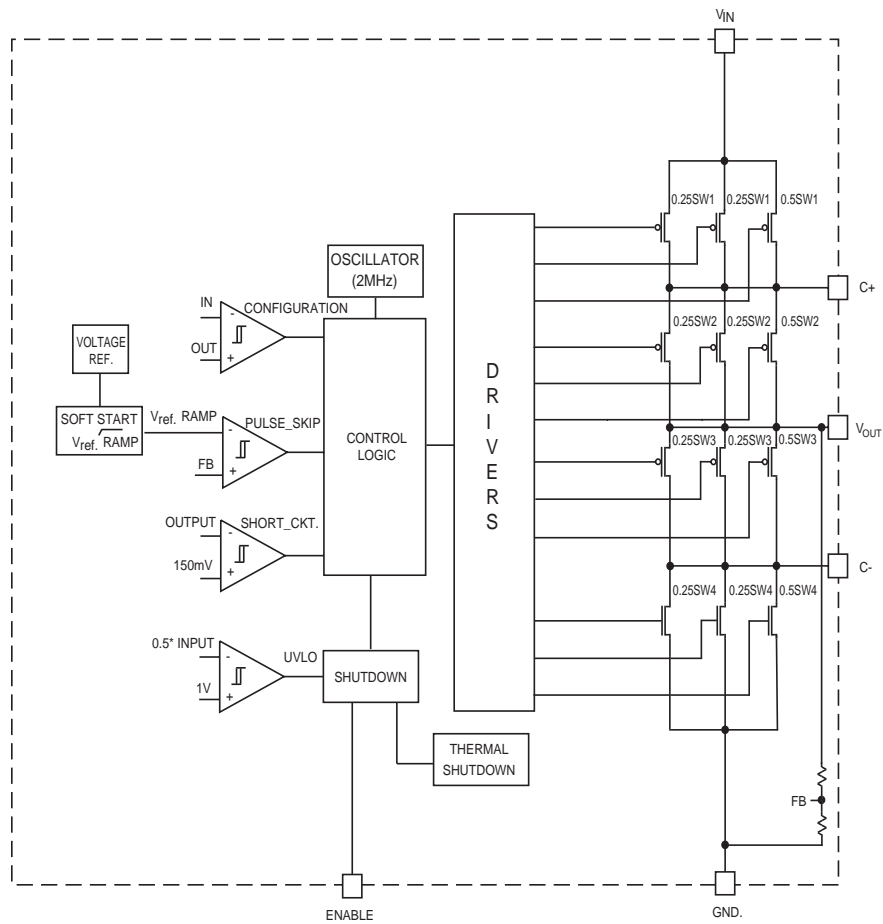


Figure 4. Block Diagram

## Detailed Description

The FAN5631/FAN5632 switched capacitor DC/DC converter automatically configures switches to achieve high efficiency and provides a regulated output voltage by means of the Pulse Frequency Modulation (PFM) pulse-skipping mode. An internal soft-start circuit prevents excessive in-rush current drawn from the supply. The switches are split into three segments. Based on the values of  $V_{IN}$ ,  $V_{OUT}$  and  $I_{OUT}$ , an internal circuitry determines the number of segments to be used to reduce current spikes.

### Step-Down Charge Pump Operation

When  $V_{IN} \geq 2 \times V_{OUT}/0.9$ , a 2:1 configuration, as shown in Fig. 5, is enabled. The factor 0.9 is used instead of 1 in order to account for the effect of resistive losses across the switches and to accommodate hysteresis in the voltage detector comparator. Two phase non-overlapping clock signals are generated to drive four switches. When switches 1 and 3 are ON, switches 2 and 4 are OFF and  $C_B$  is charged. When switches 2 and 4 are ON, switches 1 and 3 are OFF and charge is transferred from  $C_B$  to  $C_{OUT}$ .

When  $V_{IN} < 2 \times V_{OUT}/0.9$ , a 1:1 configuration, as shown in Fig. 6 is enabled. In the 1:1 configuration switch 3 is always OFF and

switch 4 is always ON. At the 1.6V output setting the configuration changes from 2:1 to 1:1 at  $V_{IN} = 3.56V$ . At the 1.3V output setting the change occurs at  $V_{IN} = 3.06V$ .

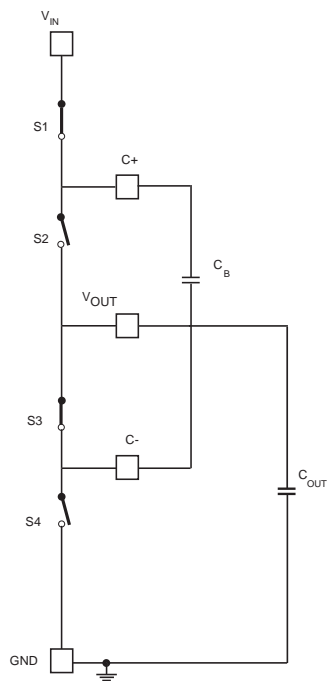
### Pulse-Skipping PFM and Fractional Switch Operation

When the regulated output voltage reaches its upper limit, the switches are turned off and the output voltage reaches its lower limit. Considering a step-down 2:1 mode of operation, 1.6V output as an example, when the output reaches about 1.62V (upper limit), the control logic turns off all switches. Switching stops completely. This is pulse-skipping mode. Since the supply is isolated from the output, the output voltage will drop. Once the output drops to about 1.58V (lower limit), the device will return to regular switching mode with one quarter of each switch turning on first. Another quarter of each switch will be turned on if  $V_{OUT}$  cannot reach regulation by the time of the third charge cycle. Full switch operation occurs only during startup or under heavy load condition, when a half switch operation cannot achieve regulation within seven charge cycles.

### Soft-Start

The soft-start feature limits in-rush current when the device is initially powered up and enabled. The reference voltage is used to

## Switch Configuration



This configuration shows the switches in the charging phase position. For the pumping phase, reverse all switch positions.

**Figure 5. Mode 2:1 Configuration**

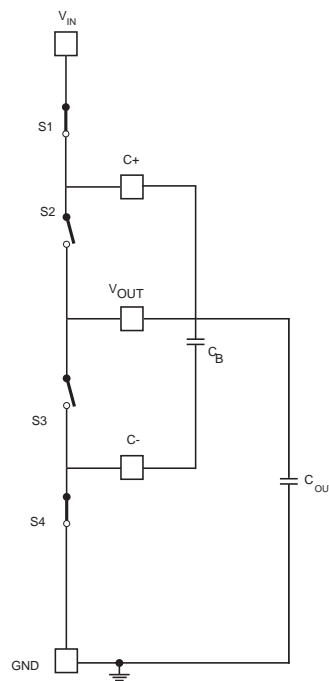
control the rate of the output voltage ramp-up to its final value. Typical start-up time is 1ms. Since the rate of the output voltage ramp-up is controlled by an internally generated slow ramp, pulse-skipping occurs and in-rush current is automatically limited.

### Shutdown, UVLO, Short Circuit Current Limit and Thermal Shutdown

The device has an active-low shutdown pin to decrease supply current to less than 1 $\mu$ A. In shutdown mode, the supply is disconnected from the output. UVLO triggers when supply voltage drops below 2V. When the output voltage is lower than 150mV, a short circuit protection is triggered. In this mode 15 out of 16 pulses during the switching will be skipped and the supply current is limited. Thermal shutdown triggers at 150°C.

### Efficiency Optimizer (FAN5632)

For higher efficiency in the FAN5632,  $V_{SEL}$  should be tied to ground to enable the efficiency optimizer feature. To achieve an optimized efficiency, the switch mode configuration transition point is shifted from a 2:1 to a 1:1 mode until the output voltage falls to 20% of its nominal value. For example, when the nominal output voltage is 1.5V, the output voltage is allowed to drop to 1.2V. This will maintain a peak efficiency of 85% for the input voltage range of 2.9V to 3.5V. For normal operation,  $V_{SEL}$  should be tied high.



This configuration shows the S1 and S2 switches in phase 1 position. For phase 2, reverse the positions of the S1 and S2 switches. The S3 switch is always OFF, and the S4 switch is always ON.

**Figure 6. Mode 1:1 Configuration**

## Applications Information

The FAN5631/FAN5632 requires one ceramic bucket capacitor in the 0.1 $\mu$ F to 1 $\mu$ F range; one 10 $\mu$ F output bypass capacitor and one 10 $\mu$ F input bypass capacitor. To obtain optimum output ripple and noise performance, use of low ESR (<0.05 $\Omega$ ) ceramic input and output bypass capacitors is recommended. The X5R- and X7R-rated capacitors provide adequate performance over the -40°C to 85°C temperature range.

The bucket capacitor's value is dependent on load current requirements. A 1 $\mu$ F bucket capacitor will work well in all applications at all load currents, while a 0.1 $\mu$ F capacitor will support most applications under 100mA of load current. The choice of bucket capacitor values should be verified in the actual application at the lowest input voltage and highest load current. A 30% margin of safety is recommended in order to account for the tolerance of the bucket capacitor and the variations in the on-resistance of the internal switches.

One of the key benefits of the ScalarPump™ architecture is that the dynamically scaled on-resistance of the switches effectively reduces the peak current in the bucket capacitor and therefore input and output ripple currents are also reduced. Nevertheless, due to the ESR of the input and output bypass capacitors, these current spikes generate voltage spikes at the input and output pins. However, these ESR spikes can be easily filtered because their frequencies lie at up to 12 times the clock frequencies. In



applications where conductive and radiated EMI/RFI interference has to be kept as low as possible, consider the use of additional input and output filtering.

### PCB Layout Considerations

While evaluating the FAN5631/FAN5632 (or any other switched capacitor DC-DC converter) the user should be careful to keep the power supply source impedance low; use of long wires

causing high lead inductances and resistive losses should be avoided. A carefully laid out ground plane is essential because current spikes are generated as the bucket capacitor is charged and discharged. The input and output bypass capacitors should be placed as close to the device pins as possible.



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E <sup>2</sup> C MOS™	i-Lo™	OCX™	μSerDes™	UniFET™
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